UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/706,157	11/03/2000	Mario Nemirovsky	P3817	5005

24739 7590 03/24/2004

CENTRAL COAST PATENT AGENCY
PO BOX 187
AROMAS, CA 95004

EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/24/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/706,157	NEMIROVSKY ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 1/2/04.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,5,6,8,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubey (patent No. 5,724,565) in view of Kimmel (patent No. 6,105,053).

1. Dubey taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Instruction source (instruction cache 110) (e.g., see fig. 1A);

b) A first cluster of a plurality of streams fetching instruction from the instruction source (e.g., see figs. 1A, 1B, col. 6 line 38-col. 7, line 55 and col. 8, lines 16-60);

b) A second cluster of a plurality of streams fetching instructions from the instruction source (e.g., see figs. 1A, 1B and col. 6, line 38-col. 7, line 55 and col. 8, lines 16-60);

c) Dedicated instruction buffers in each cluster for individual streams (e.g., see col. 7, lines 48-65 and fig.1A);

d) First dedicated dispatch stage in the first cluster for dispatching instructions to execution units (e.g., see col. 7, line 48-col. 8, lines 60);

e) Second dedicated dispatch stage in the second cluster for dispatching instructions to execution units (e.g., see col. 7, line 48-col. 8, line 60).

2. As to the limitation of the clusters operating independently with dedicated dispatch stage taking instructions only from the instruction queue in the individual cluster to which the dispatch stages are dedicated (claims 1,16), Dubey taught that each dispatcher operated independently of the other dispatchers, and in one embodiment the schedulers were split to only schedule the instructions from the corresponding dedicated dispatcher, wherein instructions were sent to the corresponding split portion of the scheduler and on to the corresponding dedicated execution units (e.g., see col. 8, lines 16-60). Also, each dispatch stage was shown (in fig. 1A) as comprising its separate instruction buffer that received instructions from the cache.

3. Dubey taught an embodiment with dispatching instructions from instruction queues (e.g., see col. 31, lines 5-24), but Dubey did not specifically detail (claim 1) that the instruction buffers that were individually dedicated to dispatchers comprised instruction queues. Kimmel however taught an individual queue and dispatcher for each execution unit (e.g., see col. 5, lines 43-58) and therefore each queue was dedicated to a dispatcher.

4. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Dubey and Kimmel. Both references were directed toward the problems of providing dynamic scheduling of instruction in chains of instruction using separate dispatchers. The addition of the separate dispatch or scheduling of groups of threads as taught by Kimmel would have allowed more efficient processing as the threads that were related would have been scheduled separately from other types of threads.

5. As per claim 2, Dubey taught execution units that are dedicated for use by individual clusters in the embodiment with split schedulers (e.g., see (e.g., see col. 8, lines 16-60). Kimmel also taught execution units that were dedicated for use by individual clusters (e.g., see fig. 1A and col. 4, lines 17-38).

6. As per claim 3, Dubey taught separate fetching from separate ports of the cache for parallel fetching to individual threads (e.g., see col. 6, line 58-col. 7,lines 65) Kimmel also taught separate cache ports parallel fetching of threads (e.g., see col. 4, lines 49-65).

As per claim 8, Dubey taught groups of execution units or functional units dedicated to each cluster (e.g., see col. 7, line 48-col. 8, line 60). Kimmel also taught grouping of functional units (e.g., JP0, JP1)(e.g., see fig.1A).

7. As per claim 5, Dubey taught means for fetching in each cycle, a series of instructions from the instruction source (cache) by a single cluster via a cache port dedicated to that cluster wherein in one cycle plural instructions are fetched for one thread of a cluster and in another cycle plural instructions are fetched for another thread of the same cluster (e.g., see col. 6, line 65-col. 7, lines 1-21).

8. As per claim 6, Dubey taught monitoring fetch program counters and fetching beginning at addresses according program counters (e.g., see col. 6, line 65-col. 7, line 21).

9. Claims 4,7, are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubey in view of Kimmel as applied to claims 1-3,5,6,8,16, above, and further in view of Tremblay (patent No. 6,343,348).

10. Tremblay taught (e.g., see fig.1) a system with eight streams executed on eight execution units and four streams per cluster (e.g., see col. 4, line 41-col. 5, line 42).

11. It would have been obvious to one of ordinary skill to combine the teachings of Dubey and Tremblay. Both systems were directed toward the problems of simultaneous independent execution of threads. One of ordinary skill would have been motivated to incorporate the Trembay teachings of independent clusters using improved register file structure with each cluster included four execution units in order to take advantage of the improved access speed to register files (e.g., see col. 3, lines 8-45).

12. Claims 9-11,13,15, are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubey (patent No. 5,724,565) in view of Kimmel (patent No. 6,105,053).

13. Dubey taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Instruction source (instruction cache 110) (e.g., see fig. 1A) ;

b) A first cluster of a plurality of streams fetching instruction from the instruction source in (e.g., see figs. 1A, 1B, col. 6 line 38-col. 7, line 55 and col. 8, lines 16-60);

b) A second cluster of a plurality of stream fetching instructions from the instruction source (e.g., see figs. 1A, 1B and col. 6, line 38-col. 7, line 55 and col. 8, lines 16-60);

c) Dedicated instruction buffers in each cluster for individual streams (e.g., see col. 7, lines 48-65 and fig.1A);

d) First dedicated dispatch stage in the first cluster for dispatching instructions to execution units (e.g., see col. 7, line 48-col. 8, lines 60);

e) Second dedicated dispatch stage in the second cluster for dispatching instructions to execution units (as per claims 9,15) (e.g., see col. 7, line 48-col. 8, line 60); and

f) Means for fetching in each cycle, a series of instructions from the instruction source (cache) by a single cluster via a cache port dedicated to that cluster wherein in one cycle plural instructions are fetched for one thread of a cluster and in another cycle plural instructions are fetched for another thread of the same cluster (e.g., see col. 6, line 65-col. 7, line 21). Dubey did not specifically that the dispatch stage was dedicated to all of the streams of each cluster. Kimmel however taught a level 3 dispatcher that dispatched instructions that were the instructions that executed on all the execution units (e.g., see col. 9, lines 29-col. 10, line 14).

14. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Dubey and Kimmel. Both references were directed toward the problems of providing dynamic scheduling of instruction in chains of instruction using separate dispatchers. The addition of the separate dispatch or scheduling of groups of threads as taught by Kimmel would have allowed more efficient processing as the threads that were related would have been scheduled separately from other types of threads.

15. As per claim 10, Dubey taught groups of execution units or functional units dedicated to each cluster (e.g., see col. 7, line 48-col. 8, line 60). Kimmel also taught grouping of functional units (JP0, JP1)(e.g., see fig.1A).

16. As per claim 11 Dubey taught fetch stage dedicated to individual streams (e.g., see col. 6, line 65-col. 7, line 21 and col. 4, lines 39-49). Kimmel also taught fetch stage

dedicated to individual streams in the cluster (e.g., see col. 7, lines 43-58 and col. 7, lines 49-67).

17. As per claim 13, Dubey taught fetching beginning at addresses according program counters (e.g., see col. 6, line 65-col. 7, line 21).

Claim Rejections - 35 USC § 103

18. Claims 12,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubey view of Kimmel as applied to claims 9-11,13,15, above, and further in view of Tremblay (patent No. 6,343,348).

19. Tremblay taught (e.g., see fig.1) a system with eight streams executed on eight execution units and four streams per cluster (e.g., see col. 4, line 41-col. 5, line 42).

20. It would have been obvious to one of ordinary skill to combine the teachings of Dubey and Tremblay. Both systems were directed toward the problems of simultaneous independent execution of threads. One of ordinary skill would have been motivated to incorporate the Trembay teachings of independent clusters using improved register file structure with each cluster accessed by four execution units in order to take advantage of the improved access speed to register files (e.g., see col. 3, lines 8-45).

21. The change in scope of the claims has necessitated a new search.

22. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

March 21, 2004

ERIC COLEMAN
PRIMARY EXAMINER